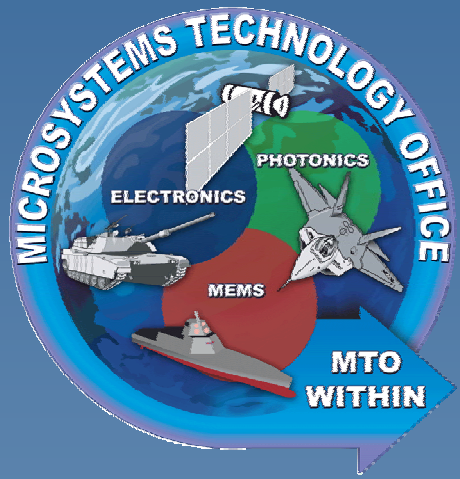
Challenges and Opportunities for InP HBT Mixed Signal Circuit Technology



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IPRM-03

Outline

- Historical Perspective on InP HBT
- DoD drivers for high performance mixed signal circuits and the underlying device issues
- Super-scaled InP HBT
- The competition: InP vs SiGe
- Summary and Projection

Heterojunction Bipolar Transistor: The Invention

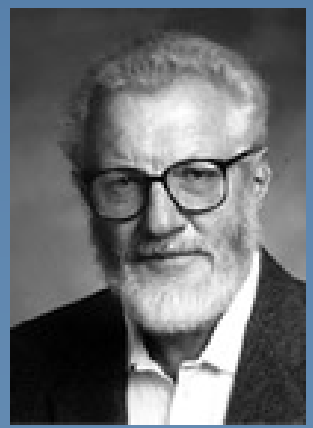
- William Shockley, US Patent 2,569,347 application June 26, 1948
- What is claimed:

1. A solid conductive device for controlling electrical energy that comprises a body of semiconductor material having two zones of one conductivity type, said two zones being contiguous with opposite faces of said zone of opposite conductivity type, and means for making electrical connection to each zone.

2. A device as set forth in claim 1 in which one of the separated zones is of a *semiconductor material having a wider energy gap* than that of the material in the other zones.

Heterojunction Bipolar Transistor: The Implementation

"The present overwhelming dominance of the compound semiconductor device field by FET's is likely to come to an end, with bipolar devices assuming an at least equal role, and very likely a leading one."

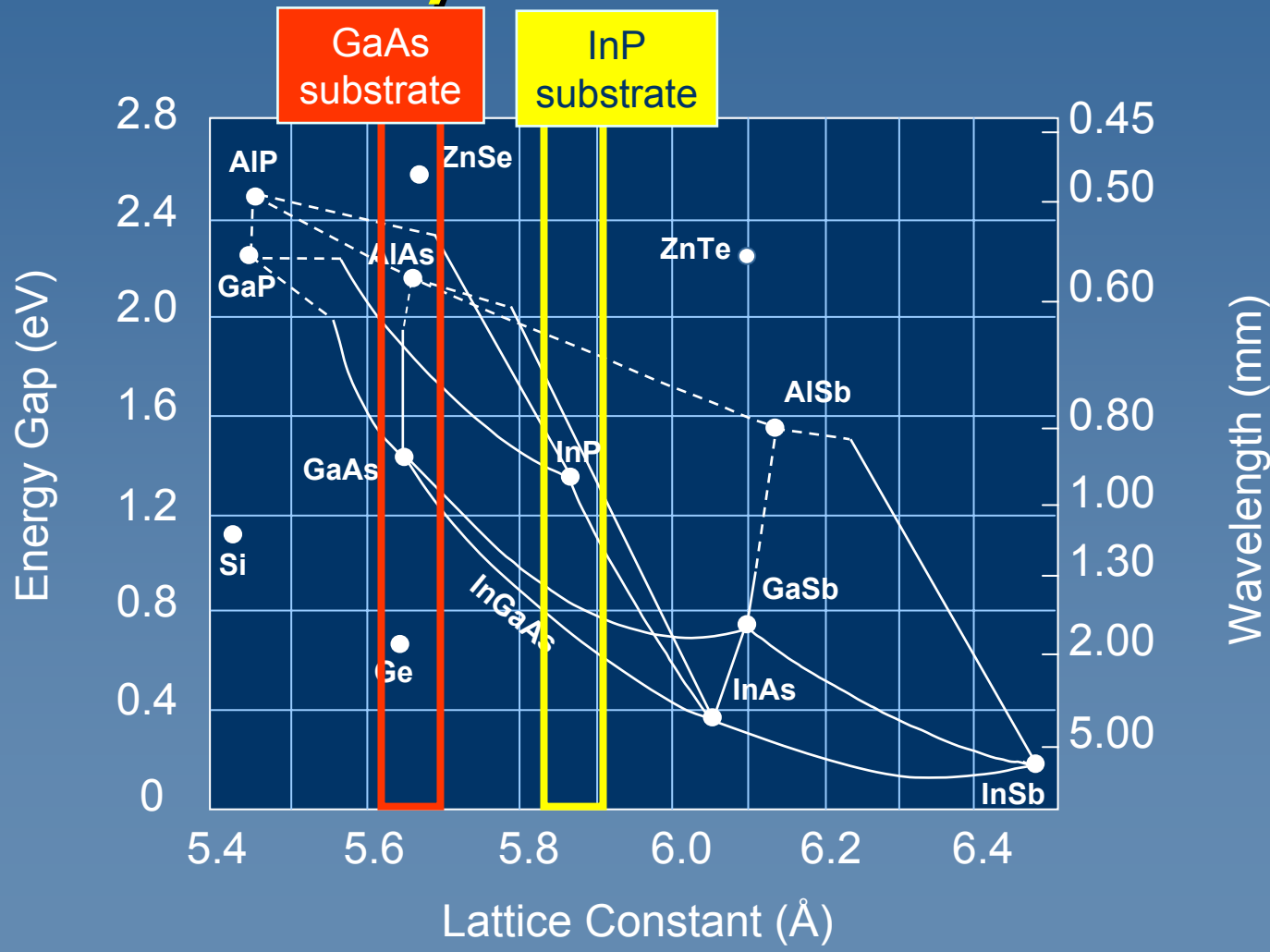


Herbert Kroemer, Proc. IEEE, vol. 70, January 1982

Kroemer's Key Aspects of HBT

- Central Design Principle: "control the forces on electrons and holes, *separate and independent from each other"*
- Wide Bandgap Emitter (claimed in W. Shockley's patent)
  - Reduce hole back injection
  - Increase electron energy
- High base doping and grading (low R_{bb} and τ_b)
- Wide Bandgap Collector
  - Increased breakdown
  - Reduced hole injection
- "Modern Epitaxy" made device structures possible
- Identified parasitic reduction as essential to optimize performance

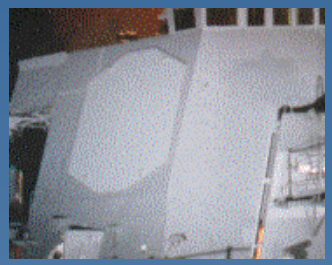
Epitaxial Layer Engineering Enabled by MBE and MOCVD



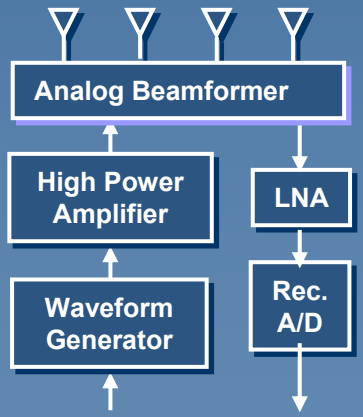
DoD Mixed Signal Circuit Drivers

Progression in RF Array Architecture and Components

Passive

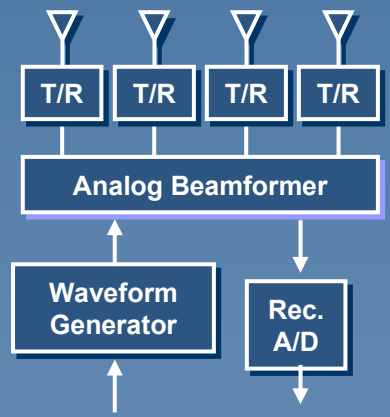


AEGIS



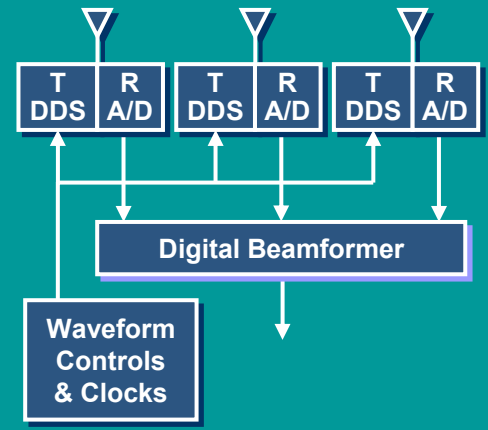
Active

F/A-18 AESA



Digital

Future systems



Increasing capability

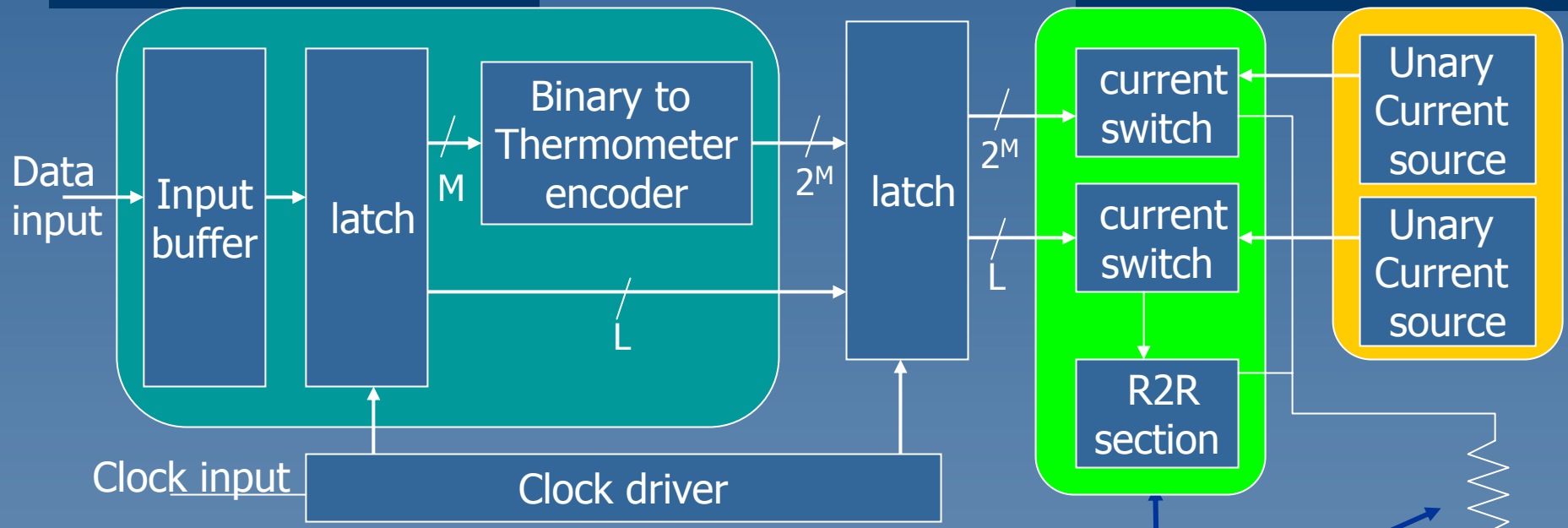
DoD Unique Mixed Signal Circuit Needs

- High center frequency
- Large bandwidth
- Large SNR
- Large spur free dynamic range
- Low power

DAC Architecture and Technology Challenges

Static Accuracy limited: Large Scale Integration and matching

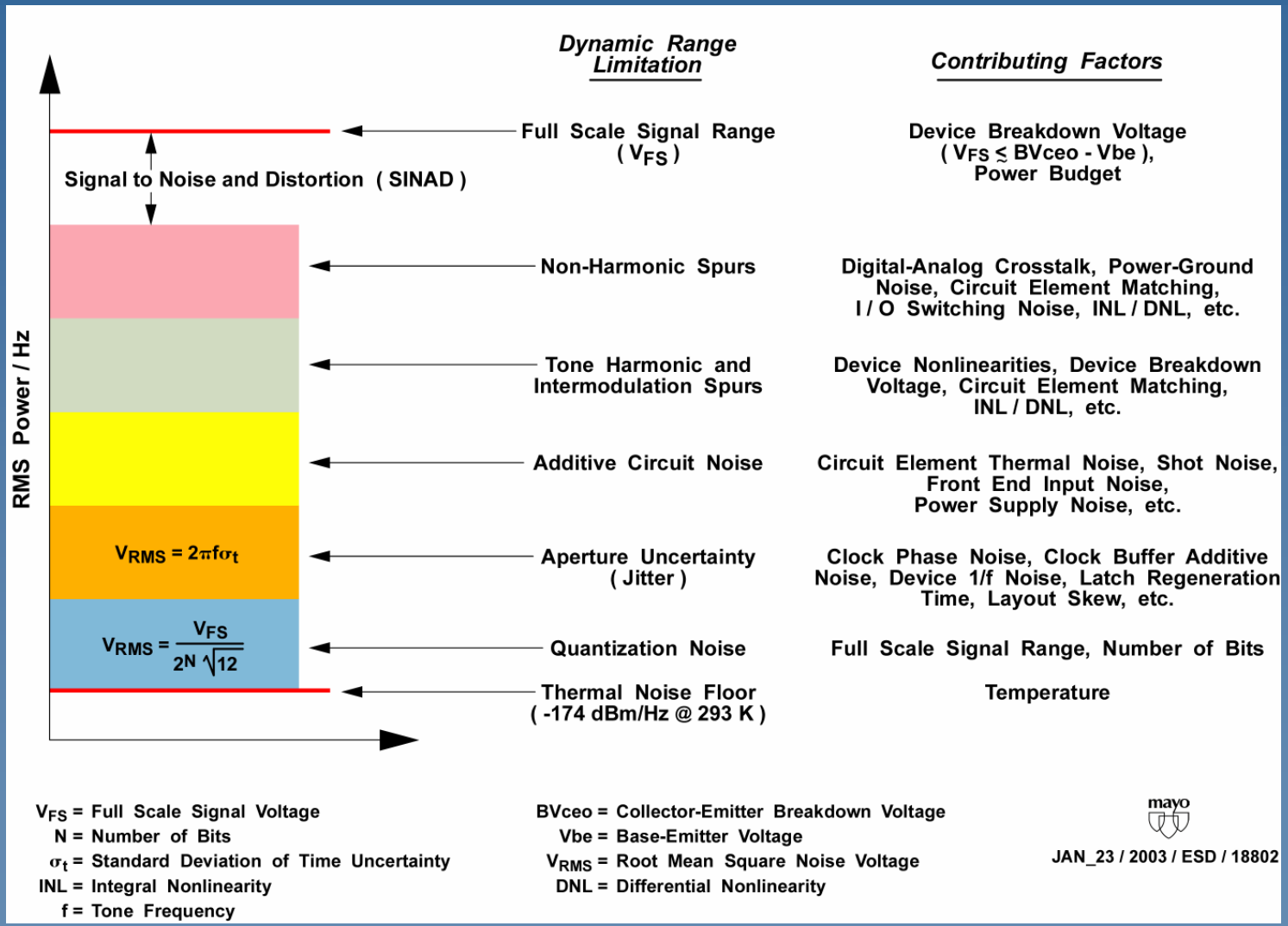
Delay limited: high F_T



Jitter Critical: High F_t and low noise

Dynamic accuracy and dynamic range limited:
Large breakdown voltage, low noise, high linearity

Circuit Dynamic Range



Performance Metrics

Digital

- Gate delay
- MIPS
- Clock speed
- DC power

Analog

- Cut off frequency
- Noise figure
- Output power
- Linearity
- DC power/PAE

Mixed Signal

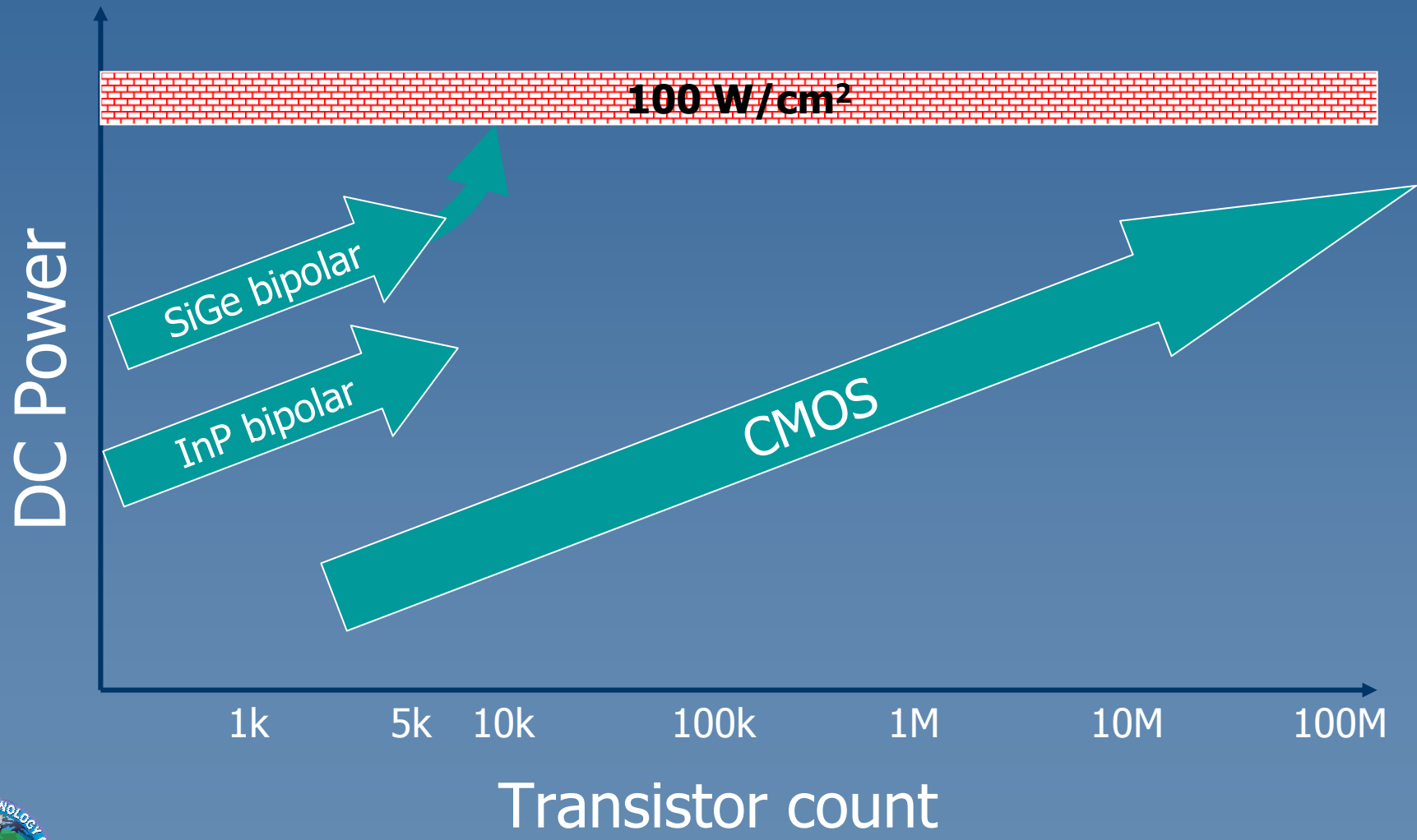
- SNR
- Bandwidth
- Sampling frequency
- Dynamic range
- DC power

No one device level metric is enough.
The only critical metric is circuit performance.

InP HBT Process Limitations to Integration and Scaling

- Subtractive processing with wet etching
- Metal lift-off processing
- Limited interconnect metallization
- Current drive
- Transistor density

Power Limitations



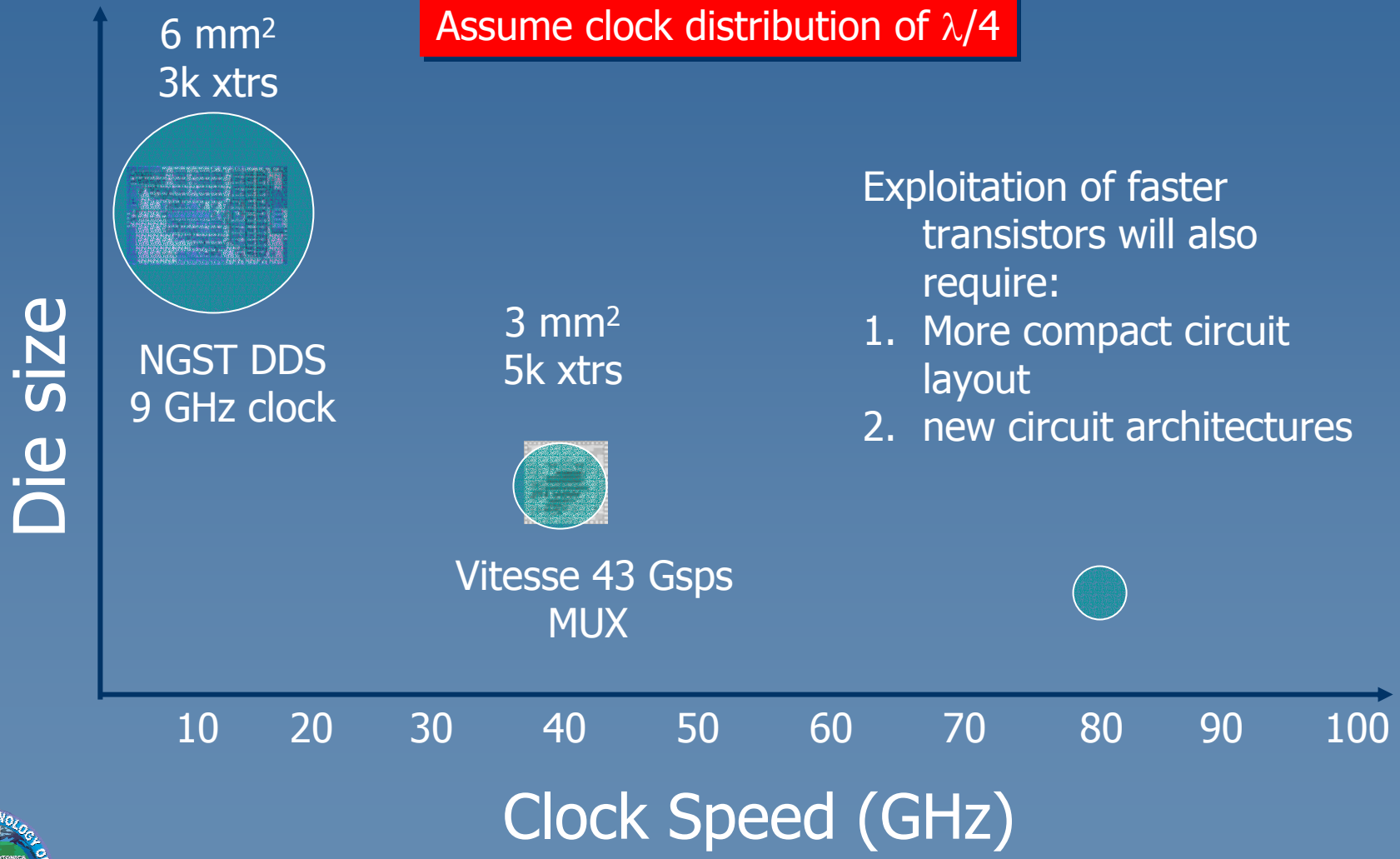
Power Limits to Integration

- Conservative Assumptions
  - Limit chip power dissipation to 100 W/cm^2 (current Pentium processor)
  - Logic swing $\geq$ 8kT = 200 mV
  - ECL (max speed) ~30 mW per MSFF
  - CML (reduced power) ~20 mW per MSFF

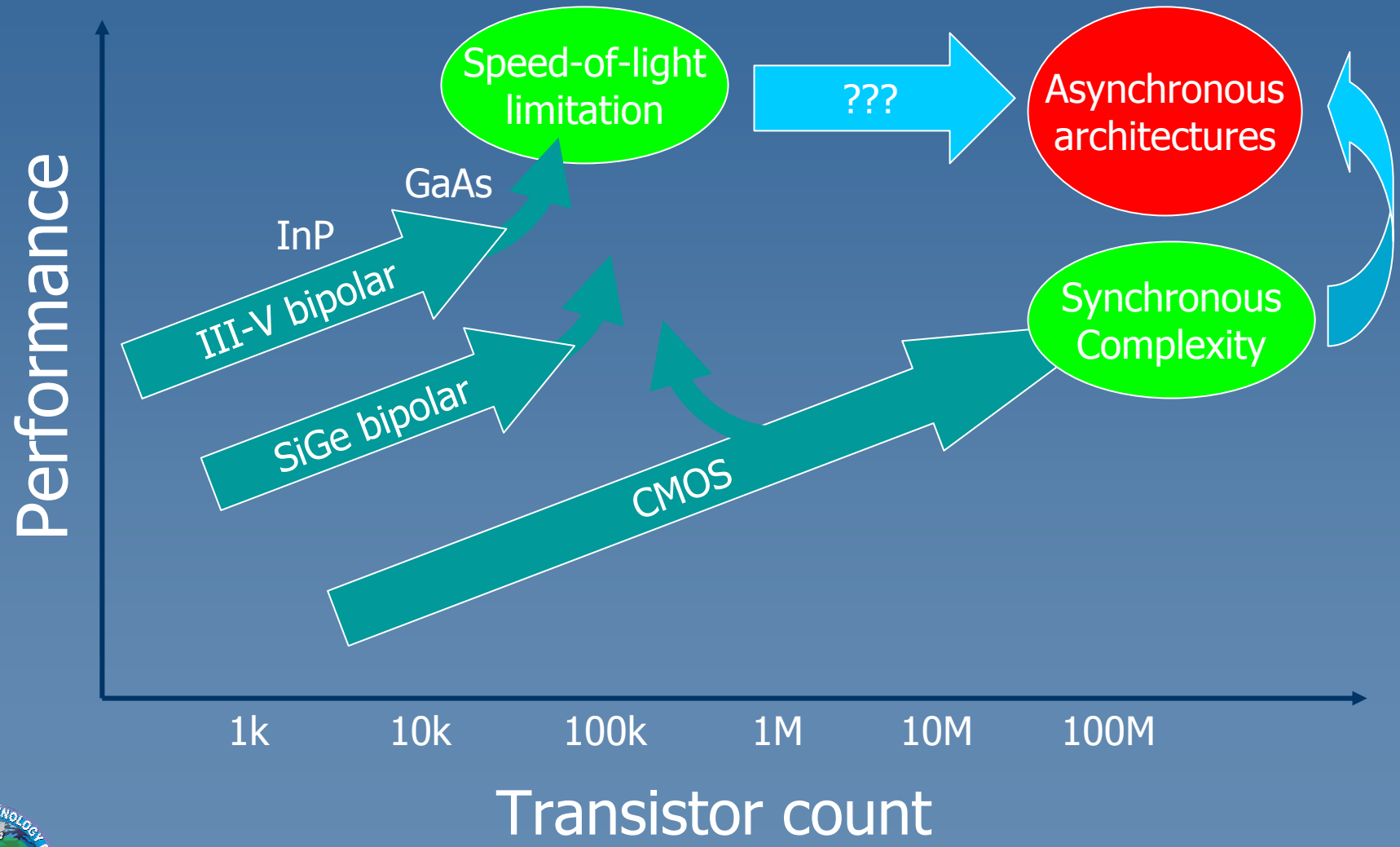
Power Limit to Integration:
~3,000 gates = 30,000 transistors

Clock Distribution Limit

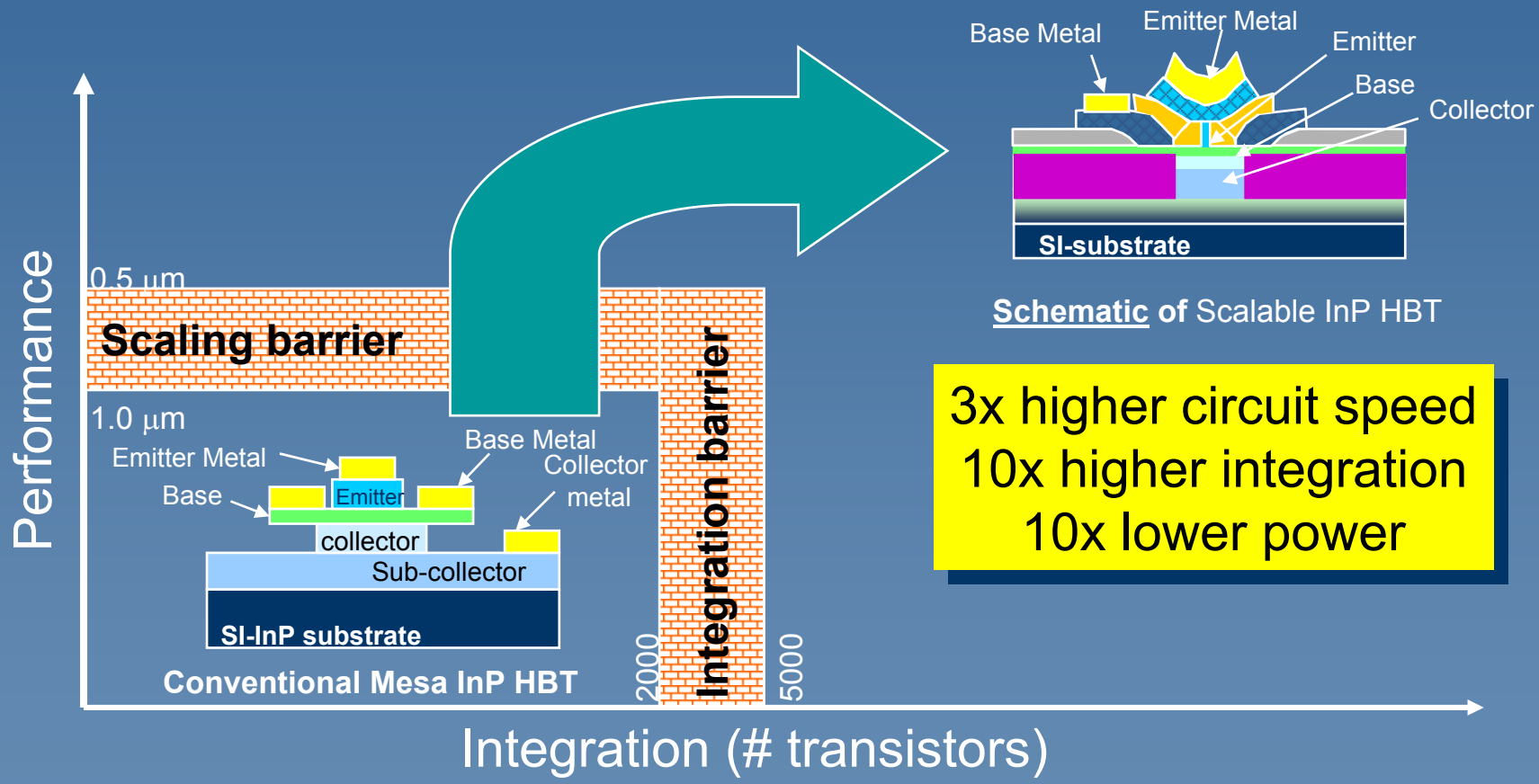
Assume clock distribution of $\lambda/4$



Synchronous Circuit Timing



Super-Scaled InP DHBTs

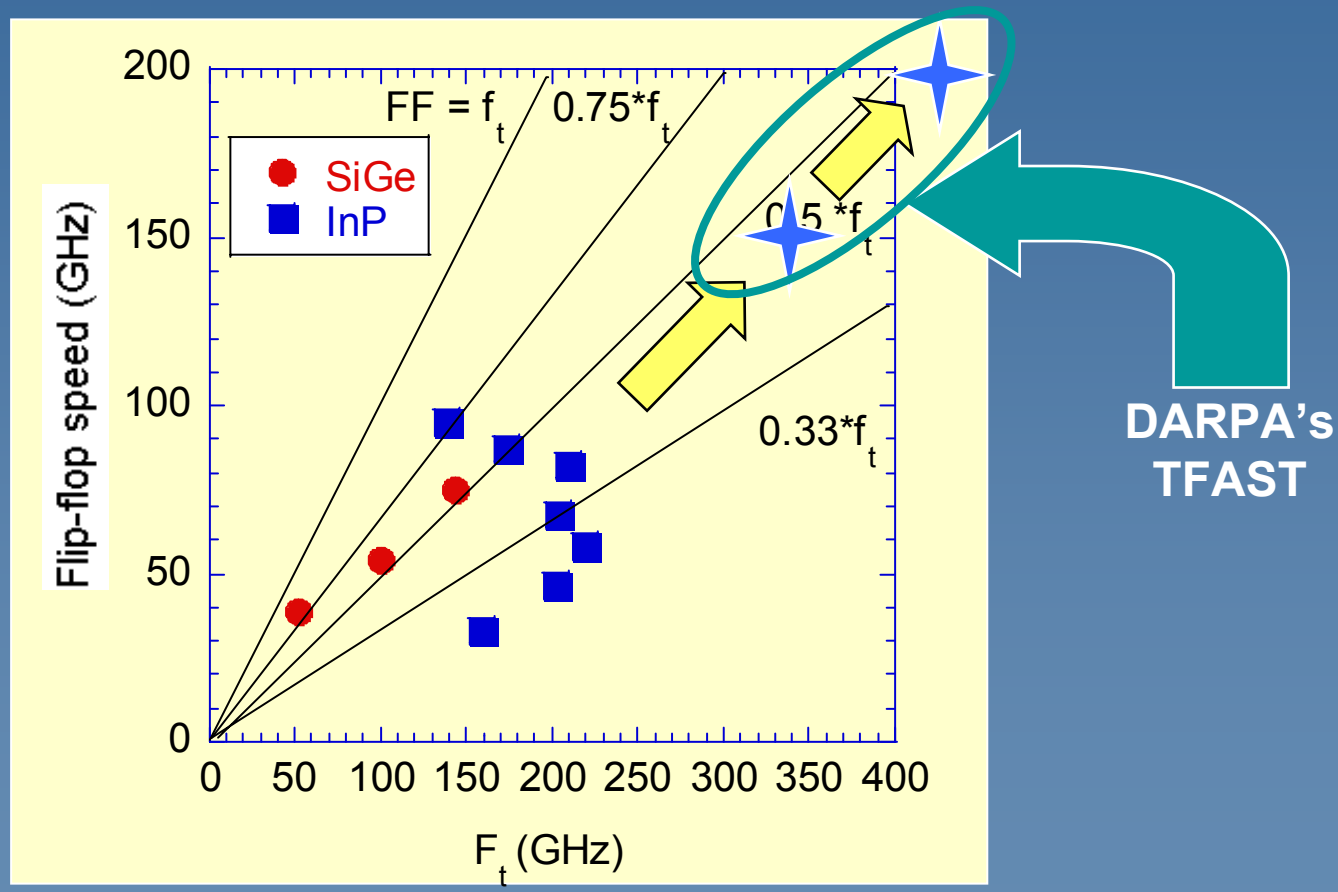


Schematic of Scalable InP HBT

3x higher circuit speed
10x higher integration
10x lower power

Super Scaled InP HBT Technology

Static flip-flop is building block for mixed signal circuits



Mixed Signal Figure of Merit: f_t is not enough

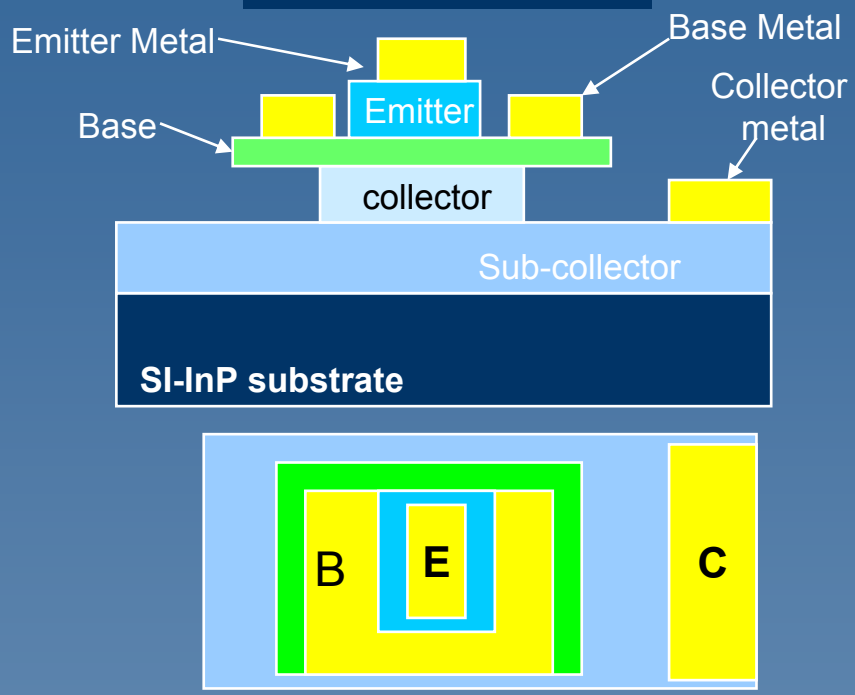
$$(1)\ f_t, f_{\max}$$

$$(2)\ \frac{J_C V_{CEO}}{C_{cb} \Delta V_{LOGIC}}$$

InP mesa HBT circuit performance is limited in J_c and C_{cb}

InP HBT Revolution

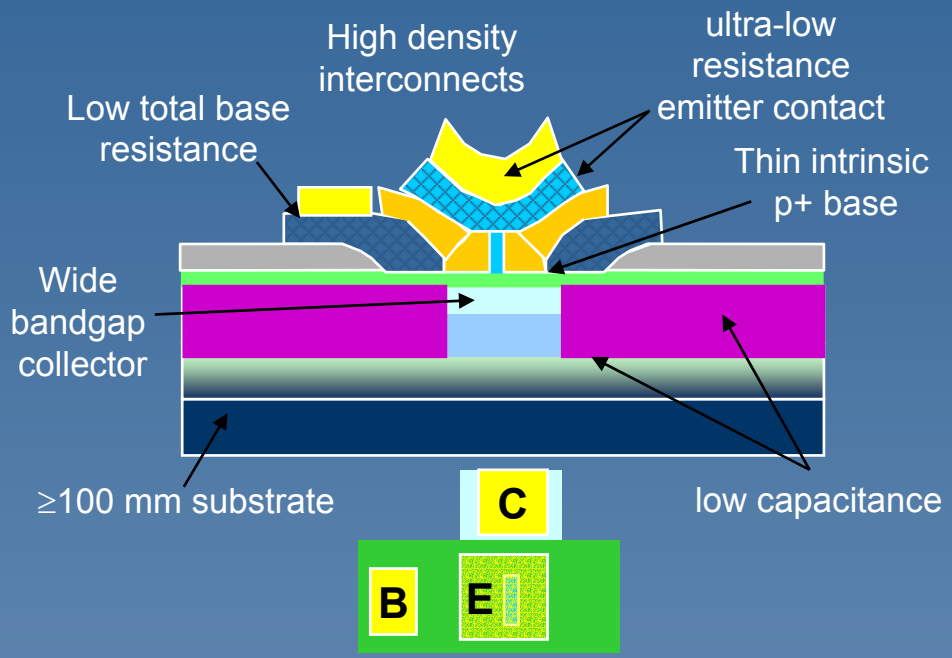
Mesa HBT today



+ Low capacitance
+ Low base resistance

- Inherent limitation on minimum feature size
- Poor thermal dissipation
- Limited emitter contact
- Limited current capability
- Process limits integration

Schematic TFAST HBT



+ Low capacitance
+ Low base resistance
+ Low emitter resistance (High J_c)
+ Scalable feature size
+ Small foot print, improved thermal
+ Planar, high integration potential

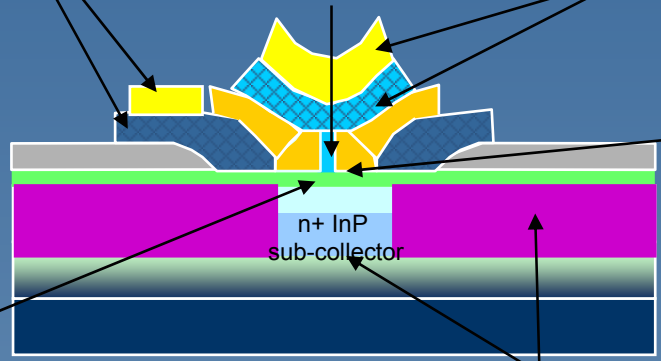
- **Paradigm shift in InP HBT technology**

Technical Challenges and Approaches for Super-scaled InP DHBT

G. Low resistance extrinsic base and base contact:
1. extrinsic MBE regrown base
2. extrinisic MOCVD regrown base
3. implant p+ link region
4. re-aligned extrinsic base
5. dielectric spacers

A. scalable emitter
1. MBE regrown emitter
2. MOCVD regrown emitter
3. side wall spacers in emitter window
4. high T base contacts

B. ultra-low resistance emitter contact:
1. graded AlInAs/InAs
2. regrown poly n++ InAs/InGaAs
3. expanded contact region

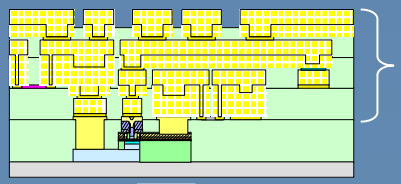


F. Epitaxy Growth Technique
1. MBE
2. MOCVD

C. thin, p+ base for high f_t/f_{max}:
1. C or Be-doped InGaAs
2. C-doped GaAsSb

E. Collector/Base band line-up:
1. GaAsSb base
2. chirped superlattice
3. doping dipole

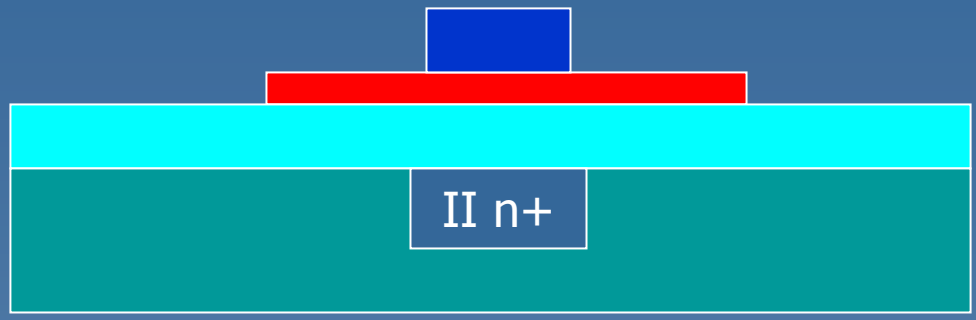
D. Selective doping regions for reduce C_{BC}:
1. ion implantation for isolation
2. Ion implantation for selective doping
3. selective regrowth or overgrowth
4. replanarized buried dielectrics



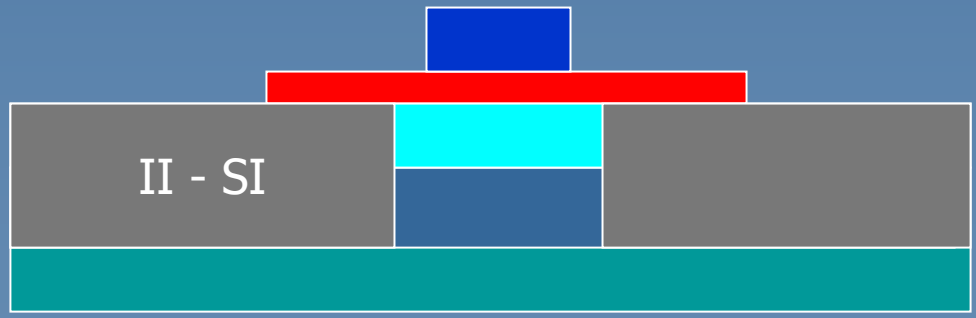
H. Interconnects for 100 GHz:
1. Si-like 4-plus level interconnects (Al or Cu) with CMP
2. spin-on dielectrics plus replanarization
3. plated Au
4. thin substrate for backside ground plane

I. Design and Test

Implanted Subcollector



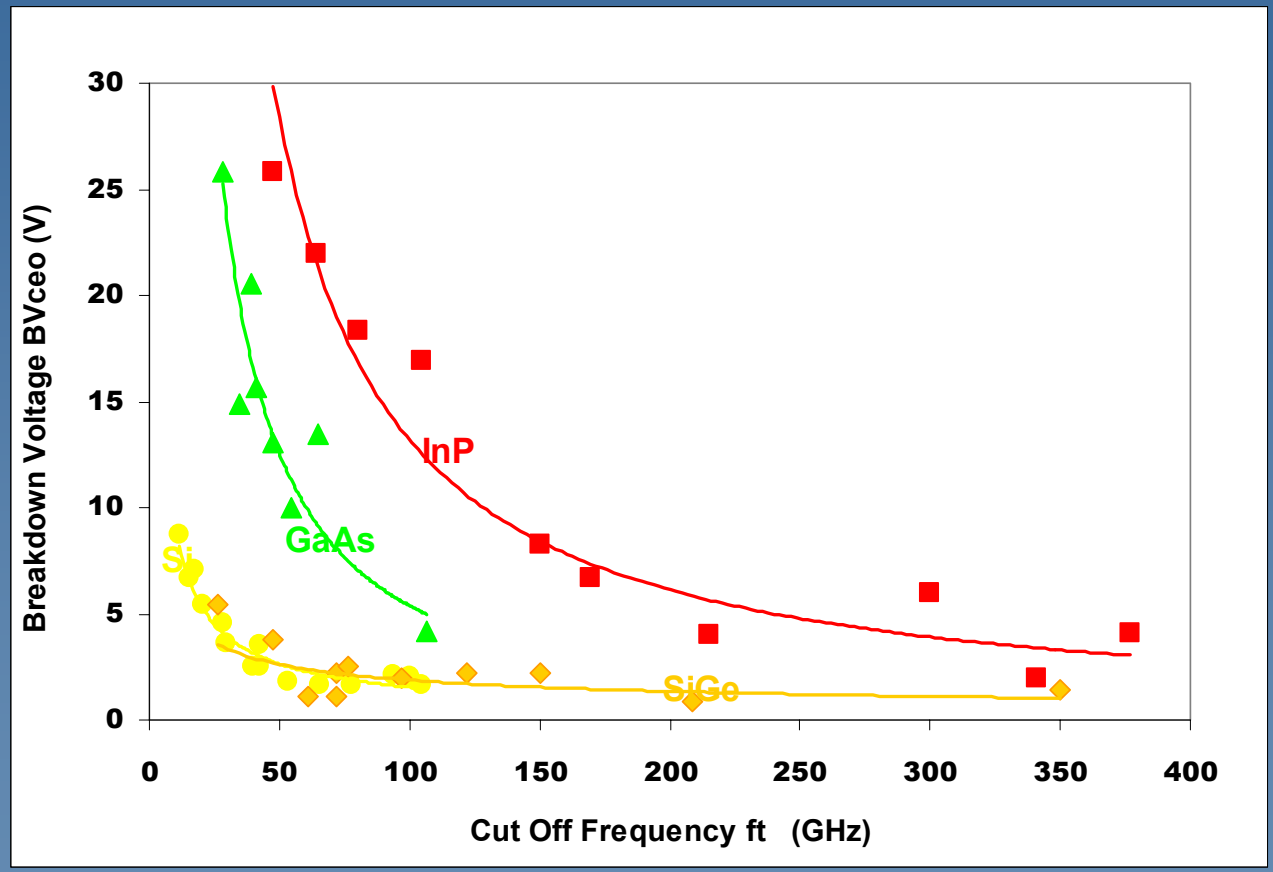
Implant Isolated Extrinsic Collector



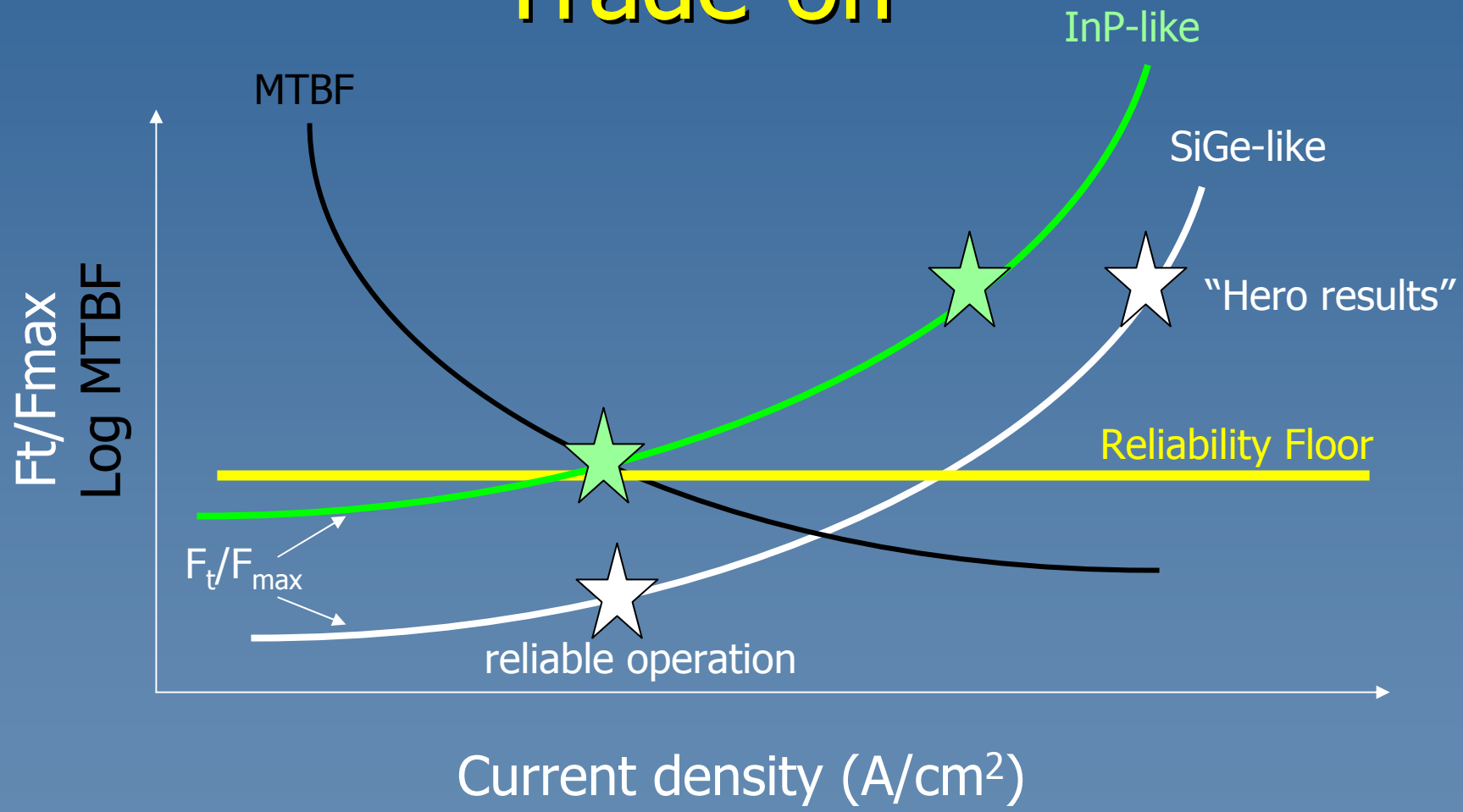
InGaAs vs GaAsSb base

	InGaAs	GaAsSb
Base p-doping (C/Be) (cm^{-3})	C: 1-2e20 Be: 1e20	C: 2e20
Base carrier lifetime	good	good?
BC Heterojunction blocking	Requires band engineering	None at low current
Best demonstrated current density (kA/cm^2)	850	500
Demonstrated growth techniques	MBE preferred	MOCVD preferred
Hydrogen passivation of Carbon	yes	Not reported

F_t versus BV_{ceo}



Performance vs Reliability Trade-off



HBT Attributes for High Dynamic Range DACs/ADCs

attribute	SiGe HBT	InP DHBT
Breakdown voltage: BVceo, BVbco	<2V, 5V	>4V, >8V
Gain at 20 GHz	22 (0.12um x11 um)	>20 dB (0.4um x 11 um MESA) >35 dB (0.4 um x 6 um TS)
Substrate cross talk	moderate	low
Linearity (Third order intercept)	good	excellent
1/f noise corner frequency	400 Hz	~ 1 KHz
20 GHz Noise Figure	1.4 dB	0.7 dB
F_t, f_{max} (best reported) (GHz)	350, 170; 270,260 (0.12 um x 2.5 um)	370, 280[1] (0.35 um x 5um); 300,300 (0.4um x 11um)
Current density at max F_t	2 MA/cm^2	0.5 MA/cm^2
V_{be} matching	excellent	excellent

[1] SHBT

Testing Challenges for 150 GHz flip-flips

- Limited sources at > 100 GHz
- Drive power at frequency
- Cable and probe losses
- Differential versus single ended

Future Applications (?)

- ADC and DAC/DDS for military radar, communications, and electronics warfare
- 40 Gbps (80/160 Gbps): it will come but when and with what requirements?
- Equalization and predistoration for analog components (OE and rf/microwave)
- Ideal RF links via digital linearization
- Low power HPA for mobile electronics
- Collision avoidance radar
- All weather W-band radar

Summary

- InP HBT *still hold* the potential for differentiating mixed signal capability
- Aggressive scaling, reduced power, and increase integration is required to achieve full potential
- Never stand still, the competition is also moving ahead fast!!

Acknowledgements

- TFAST program performers, especially:
  - Mark Rodwell, UCSB
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